REMARKS

This is in response to the Official Action currently outstanding with regard to the present application, which Official Action the Examiner has designated as being FINAL.

At the outset, Applicants thank the Examiner for the courtesy accorded to their undersigned representative during a telephone interview on 29 June 2006. As the Examiner's Interview Summary correctly indicates, during the course of the interview Applicants' Amendment of 25 April 2006 and the Kanatani et al (US 5,414,443) reference were discussed, but no agreement was reached.

Claims 1-7 and 9-24 were pending in this application at the time of the issuance of the currently outstanding FINAL Official Action. By the foregoing Amendment, Applicants have proposed the amendment of Claims 2, 3, 5, 7, 9-11, 13, 15, 17, 19, and 22. It also is proposed that Claim 1 be cancelled, without prejudice. Further it is proposed that no claims be added or withdrawn. Accordingly, in the event that the Examiner grants entry to the foregoing Amendment, Claims 2-7 and 9-24 as hereinabove amended will constitute the Claims under active prosecution in this application.

The claims of this application are reproduced above including appropriate status identifiers and showing the Amendments made as required by the Rules.

More particularly, in the currently outstanding Official Action the Examiner has:

1. Re-acknowledged Applicants' claim for foreign priority under 35 USC §119 (a)-(d) or (f), and reconfirmed the receipt of the required copies of the priority documents by the United States Patent and Trademark Office;

2. Indicated the drawing objection of 25 January 2006 has now been withdrawn – **Applicants accordingly understand that the drawings of this application now have been accepted by the Examiner.**

3. Failed to acknowledged his consideration of Applicants' Information Disclosure Statement filed in this application on 25 January 2006 by providing the Applicants with a copy of the Forms PTO/SB/08a/b that accompanied that Statement duly signed, dated and initialed to confirm the consideration of the art listed therein – **confirmation of the consideration of the Information Disclosure Statement filed on 25 January 2006 in this application is respectfully requested in response to this communication**;

4. Objected to Claims 7 and 17 on the basis of the following alleged informality:

   At Claim 7, lines 15-16 and at Claim 17, lines 22-23, the phrase "signal according to" should be changed to -- signal, in according to --;

5. Rejected Claims 1-7 and 9-24 under 35 USC 112, first paragraph, as failing to comply with the written description requirement in that the terminology "reference voltage transmission means for **simultaneously** directly transmitting multiple first voltages from external first reference voltage supply means to the reference voltage chooser circuit" lacks appropriate support in the specification as originally filed;

6. Rejected Claims 9, 10 and 19-24 under 35 USC § 112, first paragraph, as failing to comply with the written description requirement in that the terminology "a control circuit for **changing** a decoder table" lacks appropriate support in the specification as originally filed;

7. Rejected Claims 7, 17 and 18 under 35 USC § 112, first paragraph, as failing to comply with the written description requirement in that the terminology "a decoder table is **determined** by the number of tones represented by the sampling signal" lacks adequate support in the specification as originally filed;

8. Rejected Claims 1-2, 7, 11-12, and 17-18 under 35 USC § 102(b) as being anticipated by Kanatani et al. (US Patent No. 5,414,443) hereinafter "Kanatani";

9. Rejected Claims 1-2, 7, 11-12, and 17-18 under 35 USC § 102(b) as being anticipated by Fujita (US Patent No. 6,107,981, cited in PTO-892 dated 26 January 2006) hereinafter "Fujita";

10. Rejected Claims 3-6, 9, 13-16 and 19-21 under 35 USC § 103(a) as being unpatentable over Kanatani, and further in view of Hisashi (JP 10-326084), hereinafter Hisashi.

11. Rejected Claims 3-6, 9, 13-16 and 19-21 under 35 USC § 103(a) as being unpatentable over Fujita, and further in view of Hisashi (JP 10-326084), hereinafter Hisashi.

No further comment regarding items 1 to 3 above is deemed to be required in these Remarks.

With respect to item 4 above, the Examiner's comment is generally well taken. By the foregoing Amendment, Applicants propose to rephrase claims 7 and 17 so as to delete the terminology "signal according to" and replace that phraseology with --signal in accordance with--. It is respectfully submitted that the phraseology of this amendment as selected by the Applicant complies with the Examiner's suggestion, but is preferable English language phraseology to that proposed by the Examiner. Entry of this Amendment in response to this communication is respectfully requested as at least placing the present application in better form for Appeal as required by 37 CFR 1.116.

With respect to item 5, the Examiner indicates a belief that the original specification when filed did not fairly convey to one skilled in the art that applicants had in their possession the claimed feature "reference voltage transmission means for **simultaneously** directly transmitting multiple first reference voltages from external first reference voltage supply means to the reference voltage chooser circuit". In this regard, the Examiner admits that Fig. 1 discloses four connections between external reference voltage supply circuit 12 to the reference voltage chooser circuit 34 for directly transmitting four first voltages (VB1min, VB1max, and 2VB1) from the external first reference voltage supply 12 to the reference voltage chooser circuit 34, but suggests that the specification **nowhere** discloses the **simultaneous** transmission of these voltages. Applicants do not agree.

The ***simultaneous*** application of the first reference voltages to the voltage chooser circuit is inherent throughout the specification and drawings as originally filed (see particularly pages 20-25 of the specification as originally filed discussing the switches 42, the ladder resistors 36 and the voltages VB1max, VB1min and VB1). Specifically, at page 22, line 15-21 it is unambiguously stated that $VB1_{max}$ and $VB1_{min}$ are ***always*** supplied to the voltage divider circuit 35. Still further, it is clear from the drawing and the specification that $VB1_{max}$ and $VB1_{min}$ are connected directly to the voltage chooser circuit 34. Hence, since $VB1_{max}$ and $VB1_{min}$ are ***always*** supplied to the voltage divider circuit and directly connected to the voltage chooser circuit, it follows with particularity from the specification as originally filed that $VB1_{max}$ and $VB1_{min}$ are ***always (and hence "simultaneously")*** applied to the voltage chooser circuit.

With respect to item 6, the Examiner indicates a belief that the original specification when filed did not fairly convey to one skilled in the art that applicants had in their possession the claimed feature "a control circuit for **changing** a decoder table" as recited in claims 9, 10, 19 and 22. According to the Examiner's interpretation of the present specification, the control signal CS3 from the control circuit 14 is for **controlling** the decoder circuit 33 and the decoder circuit 33 can **change** the decoder table. In this regard, Applicants respectfully direct the Examiner's attention to page 15, lines 5-7 of the present specification as filed wherein it is stated that: "The **changing** of the decoder table **is controlled by** the third control signal CS3 supplied from the setup circuit 14." Applicants respectfully submit that the last quoted wording from the specification of this application as originally filed clearly supports the claim terminology indicating that the control circuit is for **changing** a decoder table.

Nevertheless, upon further consideration, Applicants have elected by the foregoing Amendment to propose that claims 9, 10, 19 and 22 be amended so as to recite: "a control circuit for ~~changing~~ controlling said decoder circuit to change a decoder table so as to change the reference voltage chosen by the reference voltage chooser circuit in ~~response to said sampled signal~~ accordance with a number of tones represented by the image signal". Specifically, Applicants believe that while the original wording of the claims is fully supported by the original specification, the Amended wording proposed hereinabove removes any possible ambiguity, and thus may be preferable to the original wording. Accordingly entry of the foregoing amendment in the latter regard in response to this communication is respectfully requested as at least placing this application in better form for Appeal.

With respect to item 7, the Examiner indicates a belief that the original specification when filed did not fairly convey to one skilled in the art that applicants had in their possession the claimed feature "a decoder table is **determined** by the number of tones represented by the sampling signal". Applicants respectfully direct the Examiner's attention to page 12, lines 11 to 16 of the specification as originally filed in the latter regard. At that point the original specification states: "The decoder circuit 33 converts the image signals to signals controlling reference voltage chooser circuits 34 in the succeeding stage using a decoder table **on the basis of the tones represented by the image signals** sampled by the sampling and latch circuits 32." Applicants respectfully submit that the foregoing wording from the original specification supports the phraseology questioned by the Examiner. (See also, page 29, line 5-8, and page 31, lines 4-7).

Upon reconsideration of the latter point, however, Applicant nevertheless has elected to proposed that the words "determined by" that were objected to by the Examiner to "indicative of" in the claims as hereinabove amended. Specifically, while it is believed accurate to state that the decoder tables are determined by the number of tones represented in the sampling signal in the sense of their original creation, it is perhaps clearer in the context of the present claims to refer not to the manner in which the decoder tables are originally determined, but rather to refer more particularly to the manner of their use in the present invention as it is proposed to be claimed hereinabove.

Turning now to the Examiner's substantive rejections as summarized in items 8 and 10 above, the Examiner has rejected claims 1-2, 7, 11-12, and 17-18 under 35 USC §102(b) as being anticipated by Kanatani et al. (US 5,414,443). In addition, the Examiner has rejected claims 3-6, 9, 13-16 and 19-21 under 35 U.S.C. §103(a) as being unpatentable over Kanatani in view of Hisashi (JP 10-326084, see English translation attached to outstanding Official Action).

More specifically, the Examiner suggests that the Kanatani reference discloses the present invention as currently claimed in Claims 1, 2, 7, 11, 12, 17 and 19. Hence, the Examiner suggests that the Kanatani et al reference discloses "reference voltage transmission means for ***simultaneously and directly*** transmitting ***the first reference voltages (VCC and VDD)***" to a voltage chooser circuit indicated at 55 (Fig. 7) from external voltage supply means. Applicants do not entirely disagree. However, Applicants strenuously disagree with the Examiner's assertion that the reference voltage chooser circuit 34 of the present invention can in any way be correctly equated to the circuit including elements 55, 72 and 76 as shown and described in the Kanatani reference with regard to Fig. 7 thereof. This is particularly the case because the lines 72 and 76 referred to by the Examiner contain analog switches (gates) that open and close alternately in Kanatani. Hence, the lines 72 and 76 of Fig. 7 of Kanatani cannot simultaneously and directly transmit first reference voltages to the voltage selector circuit 55 of Kanatani.

More particularly, in Fig. 7, the Kanatani reference illustrates a data decoder circuit, a level shifter and a D/A conversion and output circuit of the matrix liquid crystal display apparatus generally shown in Fig. 5 of Kanatani. Specifically, reference numeral 55 in Kanatani designates a voltage level selector circuit, reference numeral 7 designates a voltage signal supply circuit, reference numeral 70 designates a positive voltage signal output circuit, reference numeral 74 designates a negative voltage signal output circuit, reference numeral 79 designates a selector circuit, and reference numerals $72_0 - 72_7$ and $76_0 - 76_7$ designate analog gates. Accordingly, Applicants respectfully submit that the entirety of Fig. 7 of the Kanatani reference is the rough equivalent of the signal line drive circuit of the present invention, at least for the purposes of the present comparison. Further, for purposes of the present comparison, the reference voltage chooser circuit 34 of the present invention corresponds to the voltage level selector circuit 55 of Kanatani, while the voltage signal supply circuit 7 of the Kanatani reference roughly corresponds for the sake of comparison with the portion of Fig 1 of the present application located between the external reference power supply circuit 12 and the reference voltage chooser circuit 34.

Further, as will become apparent below, while broadly speaking the voltages V_{CC} and V_{DD} might be said to be supplied directly and simultaneously **to the entirety of the circuitry of Fig. 7 of Kanatani** in a manner similar to the supply of VB1max, VB1 min and the other VB1's supplied to the signal line drive circuitry of Fig. 1 of the present invention, Applicants respectfully submit that would be abundantly clear to anyone of ordinary skill in the art that the voltages V_{CC} and V_{DD} are ***not*** simultaneously and directly applied to the voltage level selector circuit 55 in the Kanatani reference and that this is quite difference from the input voltages VB1max and VB1min being simultaneously and directly applied to the voltage chooser circuit 34 of the present invention.

In this regard, Applicants respectfully submit that it is axiomatic that in comparing a reference to a pending claim the Examiner cannot pick and choose elements from the reference without regard for the manner in which those elements function within the reference. In other words, it is not proper for the Examiner to select only the voltage level selector circuit 55 and the inputs V_{CC} and V_{DD} via analog gates 72_7 and 76_7 of the Kanatani reference without regard to the manner of operation of the remainder of the Kanatani circuit in his attempt to justify his rejections of the currently outstanding claims of the present application. Further, Applicants respectfully submit that it also is not proper for the Examiner to disregard of the manner of operation of the Kanatani reference in a situation such as that present in this application wherein each of the reference and the pending claim define a circuit in terms of interrelated component parts. In other words, for the Examiner to simply say that Kanatani discloses a circuit that receives input voltages directly and simultaneously from external without regard for the fact that those voltages somehow under certain operational circumstances may or may not directly and/or simultaneously find their way to a particular defined portion of the overall circuit and without regard for how that occurs is not proper. To justify a finding of anticipation, the Examiner must find all of the claimed elements in a single prior art reference functioning together in the manner claimed. Applicant respectfully submits that not only has the Examiner failed to so demonstrate the anticipation of the present claims by the Kanatani reference, but also that is the present situation he cannot do so. Accordingly, Applicants respectfully submit that the Examiner cannot justify the currently outstanding rejections of the claims of this application based upon Kanatani reference and that those rejections, therefore, should be withdrawn.

In the latter regard, Applicants respectfully submit that it must be noted that the Examiner's position fails to take note of the fact that in the Kanatani et al reference, the positive and negative voltage signal output circuits 70 and 74 (that are respectively responsible for the transmission of VCC and VDD) are activated ***alternatively*** in accordance with the output from the selector circuit 79 so as to provide voltage outputs via analog gates $72_0 - 72_7$ ***or*** $76_0 - 76_7$. This mode of operation is explained in detail in the Kanatani et al reference at Column 10, line 33 through Column 12, line 29 (particularly Column 11, line 37 to Column 12, line 29) and with respect to a different embodiment at Column 14, lines 27-53. These portions of the Kanatani et al reference clearly and specifically disclose that reference voltages VCC (= $+V_7$) and VDD (= -V7) (i.e., first reference voltages provided from external) are provided to the voltage selector circuit 55 via analog gates 72_7 or 76_7, respectively, according to the control signals provided by the selector circuit 79.

Consequently, Applicants respectfully submit that it is clear that the Kanatani et al reference does not teach, disclose or suggest that ***multiple*** first reference voltages are to be provided ***directly*** (as opposed to via a controlled switch) to the voltage chooser circuit ***simultaneously*** (rather than alternatively according to which portion of the circuit is activated at any specific time by control circuit 79). At best, therefore, in Kanatani, et al. VCC is provided directly to the voltage chooser circuit via analog gate 72_7 when the circuit 7 is in one condition, and the voltage VDD is provided directly to the voltage chooser circuit via analog gate 76_7 when the circuit 7 is in its alternative condition. Therefore, there is no time during which ***multiple*** first reference voltages are provided to the voltage chooser circuit ***at the same time(i.e., simultaneously)*** as is the case in the present invention. Further, it is to be noted that the reference voltage V_c is not provided to the voltage selector circuit 55 at all.

Accordingly, it will be understood that the Kanatani et al reference indicates that in the drive circuit as shown in Fig. 7 the "power supply voltages VCC, VDD" from external are controlled by the output of the "non-inverting level shifter 794" or the "inverting level shifter 795" in the "selector circuit 79" when they are fed to the "voltage level chooser circuit 55". However, the "voltage level chooser circuit 55" ***does not directly receive both of the "power supply voltages VCC, VDD"*** (i.e., the first reference voltages) and the voltage signals V_0 to $+V_6$ or V_0 to $-V_6$ (i.e., the "second reference voltages") obtained by voltage division of the "power supply voltages VCC or VDD" ***simultaneously***. Hence, the Kanatani et al arrangement lacks the features of the present invention that allow the benefit of reduced buffer power consumption without adverse affect on the display.

In other words, in the signal line drive circuit and image display device of the present invention, the reference voltage chooser circuit receives not only the second reference voltage obtained by dividing at least two of the multiple first reference voltages, but also ***simultaneously and directly*** receives the multiple first reference voltages themselves. Hence, the reference voltage chooser circuit ***directly*** receives the multiple first reference voltages and the selected ones of the second reference voltages obtained by dividing at least two of the multiple first reference voltages ***at the same time***.

Consequently, the signal line drive circuit and image display device of the present invention includes not only voltage lines for feeding the second reference voltages obtained by dividing at least two of the multiple first reference voltages to the reference voltage chooser circuit via buffers, but also reference voltage lines for directly feeding the multiple first reference voltages to the reference voltage chooser circuit ***simultaneously***. Thus, even if, for example, the first switch is turned off to cut power supply voltage to all of the buffer circuits, the display will remain unaffected while the current consumption (power consumption) of the buffer circuits will be reduced. (see present specification at page 17, lines 12-24 and Fig. 1). Such clearly and definitely is not the case in the Kanatani et al reference.

Further, it will be understood that the same arguments that were presented in the last amendment filed in this application with respect to the Hasihi reference apply to the Kanatani et al reference. ***Indeed, the Kanatani et al reference simply represents the embodiment of the Hasishi reference discussed in the last amendment in this application that could only be achieved by the assumption that a first reference voltage passed directly through one of the buffers therein disclosed.*** The fact that the Examiner has found a reference that does not require the conjecture applied with respect to Hasishi previously does not alter the conclusion that the presently cited references ***do not teach, disclose or suggest the provision of multiple first as well as second reference voltages to the voltage chooser circuit simultaneously***.

Accordingly, it will be recalled that the present invention has the objectives of reducing power consumption in a signal line drive circuit without adverse impact upon the operating characteristics thereof; providing an image display device that utilizes that signal line drive circuit; and providing portable apparatus utilizing that signal line drive circuit. Further, Applicants have noted that to accomplish these objectives the present invention (i) eliminates an unnecessary circuit from prior art configurations, (ii) eliminates the current that would otherwise be used in the eliminated circuit, and (iii) avoids the occurrence of charging/discharging stray capacitance between bus lines when the image signal represents a small number of tones. These objectives and the manner of their accomplishment is not taught, disclosed or suggested by the Kanatani et al reference or the Hasishi et al reference taken either alone or in combination with one another.

An important technical difference between the present invention and the Hisashi reference lies in ***whether or not multiple first reference voltages from external first reference voltage supply means are provided directly to the reference voltage chooser circuit.*** In the present invention multiple first reference voltages are provided ***directly*** to the voltage chooser circuit from external first reference voltage supply means, but that in the Hisashi reference this is not the case. The reason for this lies in the difference between the techniques utilized by Hisashi and the present invention in the determination of which image tones are to be displayed (i.e., functional considerations not directly pertinent to the differences in structure between the present claims and the cited art) and in the ability of the present invention to avoid deterioration of the image to be displayed.

Accordingly, Applicants again respectfully emphasize that in the signal line drive circuit and image display device according to the present invention, the reference voltage chooser circuit is capable of ***simultaneously*** receiving not only (i) the second reference voltages obtained by dividing the first reference voltages via buffers, but also (ii) ***multiple*** first reference voltages **directly from** the external first reference voltage supply means. In other words, the reference voltage chooser circuit of the present invention can receive two different types of reference voltages in two different ways ***simultaneously***. The multiple first reference voltages each are provided directly from the external first reference voltage supply means to the voltage chooser circuit, and the second reference voltages created by voltage division from the first reference voltages are provided to the reference chooser circuit via buffers.

In Hisashi, on the other hand, no first reference voltage is provided **directly** to the voltage chooser circuit. Instead, ***a single*** first reference voltage VDD2 is provided to the voltage chooser circuit via a buffer as the voltage Vo and second reference voltages V1-V15 created by voltage division between VDD2 and ground also are provided to the voltage chooser circuit via buffers (i.e., the structure of the Hisashi reference includes buffers that respectively correspond to ***all*** of the tones of the sampled image, see, Hisashi at Claim 1, lines 3-4). Hence, as is the case with respect to the Kanatani reference, Applicants respectfully submit that the Hisashi reference also fails to teach, disclose or suggest ***multiple*** first reference voltages provided ***directly*** to the voltage chooser circuit.

In other words, even if one assumes a total pass though by the Hisashi buffers when the switches associated with the buffers are activated by VSYNC (12), the Hisashi reference teaches, discloses or suggests only a single first reference voltage from an external reference voltage supply means provided to the voltage chooser circuit via the buffer associated with SW0 in Hisashi's Fig. 3 just as Kanatani et al teaches the pass though of either VCC or VDD alternately, not together.

As mentioned above, according to the present invention, the first reference voltages supplied continuously to the voltage chooser circuit portion of the signal line drive circuit prevent the deterioration of display quality even when the first switch is OFF such that no power voltage is supplied to the buffers. This allows a reduction in the current consumption (power consumption) in the buffers. (See, page 17, lines 12-24, and Fig. 1 of the present specification). In the Hisashi device, on the other hand, the voltage chooser circuit receives input voltage only while the switch is ON. When the switch is OFF, the application of voltage, including the constant voltage VDD2, to the buffers is cut off with the result that the buffers stop operating and substantially no bias current flows therethrough. (See, Hisashi at paragraph 0009, lines 28-31) Accordingly, when the current consumption (power consumption) in the buffers is reduced in the Hisashi reference by turning the switch OFF, there is an inevitable deterioration in the quality of the display unlike the situation with respect to the present invention. Consequently, one skilled in the art would not be led to combine the Kanatani et al reference with the Hisashi et al reference in order to achieve the goals of the present invention, and even if that combination were to be made it would be unsuccessful for the intended purpose.

In addition, with specific regard to Claims 7 and 17, Applicants respectfully note that by adopting the structures herein claimed the number of bus lines to which the image signal is supplied can be reduced. This also allows for the reduction of the power required by the device (i.e., reduces power consumption) according to the number of tones required for the transmission of the data via the bus lines.

Also as stated previously, a main feature of Claim 7 is that ***a decoder circuit*** controlling the reference voltage chooser circuit ***is controlled through a third control signal to change a decoder table determined by the number of tones represented by a sampling signal generated by a sampling of the image signal***, whereby the reference voltage chooser circuit changes a reference voltage choosing pattern of the signal line driving circuit. Claim 17 incorporates these features into the display device therein claimed. In either case, however, it will be understood that as emphasized above with regard to the Examiner's enablement and written description rejections, in the present invention the decoder table used can be changed in accordance with the number of tones represented by the image signal. Consequently, the signals transmitted by the bus lines may be fixed when the image signal represents a small number of tones. This fixation prevents the occurrence of the charging/discharging of stray capacitances between the bus lines thereby also reducing the power consumption of the signal line driving circuit. This feature also is neither taught, disclosed nor suggested by either the Kanatani et al reference, or the Hisashi et al reference, or any combination thereof.

More particularly, conventionally in cases where for example 6 bus lines are provided (i.e., a 6 bit mode), signals indicative of "1" and "0" need to be supplied to all six bus lines so as to express "white" or "black". In cases wherein 6 bus lines are provided in the context of the present invention as claimed in Claims 7 and 17, however, a signal indicative of "1" or "0" has to be supplied to only one bus line so as to express "white" or "black" while the signals supplied to the other bus lines can remain fixed to "0" or "1". Neither the Kanatani et al nor the Hisashi reference, teach, disclose or suggest a structure for "reducing the number of bus lines to which the image signal is supplied or a structure for reducing power consumption equivalent to that presently claimed in Claims 7 and 17.

Therefore, it will be understood that a main feature of the present invention is that the claimed structure includes reference voltage supply means ***directly*** inputting (i.e., directly transmitting without the intervention of other circuit elements) ***multiple*** first reference voltages supplied by external first reference voltage supply means to a reference voltage chooser circuit. With that arrangement, no buffer circuit is required for the reference voltage line(s) directly transmitting the first reference voltages. Therefore, the signal line drive circuit takes up a smaller area and eliminates the amount of current that would otherwise be utilized by buffer circuits associated respectively with the first reference voltages. This results in power savings by the claimed signal line drive circuit in comparison to the prior art.

In addition, when second reference voltages are provided to the voltage chooser circuit via buffers, those second reference voltages are provided to the voltage chooser circuit ***simultaneously*** with the first references voltages whereby the voltage chooser circuit can effectively choose among them according to the decoder table then in use.

As mentioned briefly above, a claim is anticipated only if ***each and every element*** as set forth in the claim is found either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) Applicants respectfully submit that this clearly is not the case here.

Similarly, with respect to Section 103 of Title 35 United States Code, it is settled that:

> "To establish a *prima facie* case of obviousness under Section 103, Title 35 United States Code (35 US §103), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference (or references when combined) must teach or suggest all of the claim limitations***. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2D 1438 (Fed. Cir. 1991)."

Manual of Patent Examining Procedure §2142 (8th Edition), at page 2100-2121, *et seq.*

Applicants respectfully submit that it has been incontrovertibly demonstrated above that the Kanatani reference purely and simply does not contain, disclose, teach or suggest all of the limitations of the present claims, and further that the Examiner's attempt to avoid the requirement that all of the claimed elements be shown in the prior art by lumping all, or a substantial part of, the elements of the Kanatani reference together is simply unsatisfactory from the point of view of justifying the currently outstanding rejections. Applicants respectfully submit that all of the elements means all of the elements as set forth in the claims, not some lump sum grouping thereof.

In addition, with respect to items 9 and 11 above, Applicants respectfully call the Examiner's attention to the fact that it is proposed by the foregoing Amendment that all of the independent claims of this application be amended so as to indicate that first reference voltages and a second reference voltage produced by dividing the first reference voltages utilizing ladder resistor are supplied to the reference voltage chooser circuit, and that switches that are controlled by a control signal are interposed between the ladder resistor and the respective power supply lines for the first reference voltages. Support for these amendment is found in the original specification at page 19, line 8 to page 24, line 9.

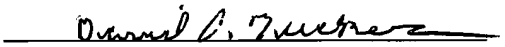
Applicants respectfully submit that neither the Fujita reference nor the Hisashi reference teach, disclose or suggest either producing a second reference voltage by dividing first reference voltages utilizing ladder resistor or interposing switches controlled by a control signal between the ladder resistor and the respective power supply lines for the first reference voltages. Accordingly, Applicants respectfully submit that the Examiner's rejections based upon the Fujita or the Fujita and the Hisashi references in combination are overcome by the foregoing references as well thereby placing this application in condition for allowance.

For each and all of the foregoing reasons, Applicants respectfully submit that the claims of this application as they will stand upon the entry of the foregoing Amendment now are in condition for allowance. Therefore, reconsideration and allowance of this application in view of the foregoing Amendment and Remarks is respectfully requested in response to this communication.

Applicant also believes that additional fees beyond those submitted herewith are not required in connection with the consideration of this response to the currently outstanding Official Action. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge and/or credit Deposit Account No. 04-1105, as necessary, for the correct payment of all fees which may be due in connection with the filing and consideration of this communication.

Respectfully submitted,

Date: September 11, 2006



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Application No. (if known): 09/925,909 Attorney Docket No.: **56377-RCE (70904)**

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